High Capacitive Density Stacked Decoupling Capacitor Structure

ABSTRACT OF THE DISCLOSURE

[0026] A capacitive structure (10). The capacitive structure comprises a semiconductor base region (30) having an upper surface, a well (12) formed within the semiconductor base region and adjacent the upper surface, a first dielectric layer (38) adjacent at least a portion of the upper surface, and a polysilicon layer (16) adjacent the first dielectric layer. The well, the first dielectric layer, and the first polysilicon layer form a first capacitor and are aligned along a planar dimension. The capacitive structure further comprises a first conductive layer (20_1) positioned with at least a portion overlying at least a portion of the polysilicon layer, a second dielectric layer (20_2) adjacent the first conductive layer, and a second conductive layer (20_3) adjacent the second dielectric layer. The first conductive layer, the second dielectric layer, and the second conductive layer form a second capacitor and are aligned along the planar dimension.